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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,389	11/04/2003	William L. Oberlin	200312376-1	5790

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EXAMINER	
DINH, SON T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/700,389	OBERLIN ET AL.	
	Examiner	Art Unit	
	Son T. Dinh	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-15* is/are allowed.

6)☒ Claim(s) *1-7,9,10,16,18-23,26,27 and 29* is/are rejected.

7)☒ Claim(s) *8,17,24,25 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/4/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *East search hsitory*.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7, 9-10, 16, 18, 19-23, 26 and 29 arerejected under 35 U.S.C. 102(b) as being anticipated by Chu et al (U.S. Patent No 5,996,880).

Regarding claim 1, 10, 16, 19, Chu et al disclose a circuit board (10, figure 4) having front (20, 22, 24,26 in figure 4mounted in front surface) and back surfaces (40, 42, 44, 46 in figure 4 are mounted on the back surfaces; also see column 6, lines 35-40); at least one memory device (20, 22, 24, 26) having a plurality of pins (inherently included in Chu et al, since every chip must have pins so as to connect to the PCB) mounted on the front surface (as explained above) of the circuit board (10); at least one other memory device (40, 42, 44, 46) having a plurality of pins (see explanation above) mounted on the back surface (the surface that 40, 42, 44, 46 are mounted) of the circuit board (10); said memory devices being mounted on the circuit board such that at least some pins from the one memory device align with at least some pins of the other memory device to provide aligned pin pairs (see figures 3 and 4); and a via (66, figure 7) disposed in the circuit board and extending between and connecting individual pins of an aligned pin pair. Also, the address means and control means (as claimed in claim

16) are inherently included in Shu et al, since the address signal and RASO and RAS1 in figure 3 must be driven by a decoder and a controller (as recognized in the memory art)

Regarding claim 2, figure 7 of Chu et al discloses multiple vias (62, 64, 66, 68) disposed in the circuit board and extending between and connecting individual pins of different aligned pin pairs.

Regarding claims 3, 6, at least one of vias 62, 64, 66, and 68 is used to transmit address signal 54 in figure 3.

Regarding claims 4, 7, at least one of vias 62, 64, 66, 68 carries control signal (either 50 and 52 in figure 3)

Regarding claim 5, the applicant is referred to the rejection of claims 3 and 4 for the reasons of this rejection

Regarding claim 9, elements 30 and 32 in figure 4 are capacitors.

Regarding claim 18, the capacitors in Chu et al is used for providing decoupling Function (see column 10, lines 29-31)

regarding claim 20, the applicant is referred to the rejection of claims 1 and 10 for a memory controller as claimed in this claim.

Regarding claims 21-23, figure 3 of Chu et al clearly shows that their memory is dual bank configuration, and dual row.

Regarding claim 26, the memory device in Chu et al is a SDRAM (see column 9, lines 64-68)

Regarding claim 29, column 10, lines 29-31 states that the capacitors used in Chu et al PCB are decoupling capacitors.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chu et al .

Chu et al applied as above. The only difference between Chu et al and claim 27 is Chu et al is silent on the act of mounting a DDR SDRA in a circuit board. However, such act of mounting would have been obvious since it is well known in the art that the technique of mounting of SRAM and a DDR SDRAM on a circuit is the same.

Allowable Subject Matter

Claims 11-15 are allowed.

Claims 8, 17, 24-25, 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fail to teach or suggest a memory device having a circuit board, a first memory device, a second memory device, wherein both memory devices are mounted of the front and back surface of the circuit board, a memory controller mounted on the circuit board, wherein a first group of address pins are interconnected with the memory controller using a first topology and a second group of address pins are interconnected with the memory controller using a second different topology (claim 11); the particular connection of a resistor (or a termination means as claimed in claim 17) on the circuit board (claims 8,17 and 28); an interconnected branched t-topology and a daisy chained topology (claims 24-25) .

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

-Chiou et al disclose a memory device having a circuit board.

-Chu et al disclose a memory device having a circuit board.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son T. Dinh whose telephone number is 571-272-1868. The examiner can normally be reached on Monday to Friday 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Dinh
March 20, 2006

Son T. Dinh